AMENDMENTS TO THE SPECIFICATION

Please add and/or amend paragraphs as follows.

[0014.1] Figure 2C illustrates another embodiment of an imager sensor array.

[0019] Figure 7 is a flow diagram illustrating one embodiment of a method of estimating the excess ~~charge~~ signal and compensating for the excess signal in an imaging system.

[0020] Figure 8 is a flow diagram illustrating one embodiment of a method of estimating the excess ~~charge~~ signal using one reference image frame, and compensating for the excess signal in an imaging system.

[0021] Figure 9 is a flow diagram illustrating one embodiment of a method of estimating the excess ~~charge~~ signal using two reference image frames, and compensating for the excess signal in an imaging system.

[0040] Figure 2A illustrates one embodiment of an imaging system. Imaging system 2 includes a computing device 4 coupled to an imager sensor array 16. Imager sensor array 16 may be, for example, an amorphous silicon organic semiconductor TFT or diode-switched array imager. As previously discussed in relation to Figures 1A and 1B, imager sensor array 16 functions by accumulating charge on capacitors generated by pixels of p-i-n photodiodes (amorphous silicon or organic semiconductor) with scintillators or by pixels of biased photoconductors. Typically, many pixels are arranged over a surface of imager sensor array ~~19~~16 where, for example, TFTs (or single and/or double diodes) at each pixel connect a charged capacitor to charge sensitive amplifier 19 at the appropriate time. Charge sensitive amplifiers 19 drive analog to digital (A/D) converter 17 that, in turn, converts the analog signals received from amplifiers 19 into digital signals (e.g., S_T, S_E) for processing by computing device 4. A/D converter 17 may be coupled to computing device 4 using, for example, I/O device 10 or interconnect 14.

A/D converter 17 and charge sensitive amplifiers 19 may reside within computing device 4 or imager sensor array 16 or external to either device.

[0061] Figure 7 is a flow diagram illustrating one embodiment of a method of estimating the excess signal S_E 235 output from A/D converters 19 (representative of Q_E 35 in a pixel of a frame captured by the imager sensor array 16), and compensating for the excess signal S_E in the pixel of the captured frame. It should be noted that the method described herein may be implemented by the computing device 4 to generate the excess signal S_E 235. The integration time is determined based on the frame rate, step 700. As demonstrated with Figure 6, integration time is the reciprocal of the frame rate. One skilled in the art will recognize that integration time is also used for methods other than integration.

[0062] The method determines a value for K as discussed, for example, above in relation to Figure 5, step 710. In step 720, an estimation of the excess signal S_E 235 composed of linear and non-linear background signal S_{NL}, and/or non-linear lag signal S_{LAG}, based on the constant (K) value and the frame rate, is calculated. In one embodiment, the excess signal S_E 35 may be calculated, for example, by integrating $I_E(t)$, with the determined value of K, over the integration time (T)(the reciprocal of the frame rate), as described above with respect to Figure 4. In another embodiment, the excess signal S_E 235 may be calculated by summing $I_E(t)$ over a series of steps. In step 730, the estimation of excess signal S_E 235 is subtracted from a measured signal S_T 236. The measured signal S_T 236 is, for example, representative of the measured charge Q_T 36 read out of a node 34 of Figure 2B at an appropriate time and contains contributions from the charge stored on capacitor 28, also in Figure 2B, as well as non-linear charge contributions (excess ~~current~~ charge 35) from TFT 32 if the frame rate is below 20 seconds per frame, see Figure 1. The result from step 730 includes an estimation of the excess signal S_E 235 arising from radiation incident on photodiode 26a from one or more prior frames that constitutes a lag contribution. In an alternative embodiment, the processor 6 may use a look-up table storing excess signal S_E 235 estimates versus integrated time values based on frame rates.